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Development of a ReadOutDriver (ROD) for ATLAS micromegas

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ABSTRACT

Microstructured gaseous detectors are a possible replacement technology for the inner part of the forward muon spectrometer of the ATLAS detector, when the luminosity of the LHC will increase beyond the design value. During the shutdown 2011/2012, several small micromegas detectors have been installed in ATLAS between the inner tracker and the calorimeter as well as on the small wheel section. To read out these detectors along with the other ATLAS systems, a readout driver has to be developed, that integrates this subsystem into the ATLAS data acquisition infrastructure, including the trigger handling, slow control, event building and data formatting.

1. Introduction to micromegas at LHC

Future LHC upgrades will increase the luminosity by a factor of 5 at least. Accordingly the background radiation in the ATLAS detector cavern will increase. The current implementation of the small wheel precision muon tracking system will not be able to maintain its full performance under these conditions. The preferred replacement technology for the small wheel is micromegas [1] detectors, high-rate capable planar gaseous detectors.

During the 2011/2012 shutdown, several small Micromegas prototype detectors of 9 cm × 4.5 cm and 9 cm × 9 cm, have been installed in the ATLAS detector. One detector, consisting of two active layers, is located in the Minimum Bias Trigger Scintillator (MBTS) region between the inner tracker and the calorimeter; four chambers are positioned on the small wheel, close to a Cathode Strip chamber (CSC, to be replaced in future).

To read out the data from these detectors, along with all other ATLAS subsystems, a ReadOutDriver (ROD) is currently built, that includes the micromegas in the ATLAS data acquisition chain. All necessary infrastructure like a separate ReadOutSystem (ROS) PC, power supplies, cables and optical fibers have been installed.

2. The SRS system

The Scalable Readout System (SRS) has been developed within the RD51 [2] collaboration at CERN. It is a powerful and flexible platform for detector readout and control, based on modern Xilinx Virtex5 and Virtex6 [3] FPGAs (see Fig. 1). In its current configuration at ATLAS, 19 APV25 chips will be read out, using two ADC and FrontEndConcentrator (FEC) cards to digitize the analog data. A Scalable Readout Unit (SRU) will receive the FECs event data and perform the event building and data formatting, according to the requirements of the ATLAS ROS.

3. Functionalities of a ROD and their implementation in the SRU

The SRU of the SRS system will have to act like all other ATLAS RODs to maintain data acquisition compatibility (see Fig. 2). The tasks include:

3.1. Trigger, timing and control reception

The SRU board is equipped with a standard TTCrx receiver ASIC, developed at CERN. It allows direct connection to the Central Trigger Processor (CTP) via optical fiber and the synchronization to the LHC machine. Each Level1 trigger (which occurs with up to 100 kHz) sent from the CTP via the Trigger, Timing and Control network (TTC), has to be answered by the RODs. Since the readout of a single time bin from the APV25 chip takes roughly 4 μs and it is desired to read 10–20 consecutive time bins to gather relevant timing information, not every Level1 trigger can be processed in the current configuration. For this reason, the event builder generates empty events with just header and trailer for every unprocessed trigger.

3.2. Data reception

For each accepted Level1 trigger, the APV25s charge information must be obtained from the FEC cards. This will be done using the so-called DTC links, which allow a data transmission rate of 1 GBit/s using cat7 network cables. The first version of this link

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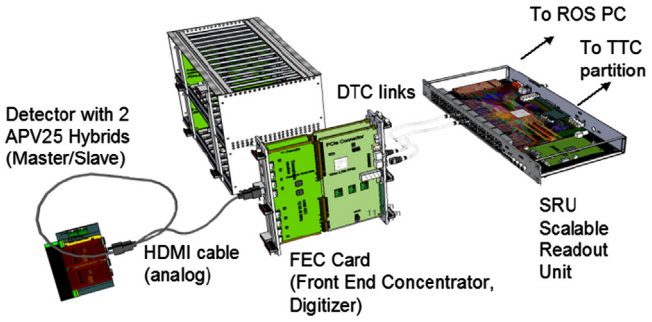

Fig. 1. The SRS system with its components.

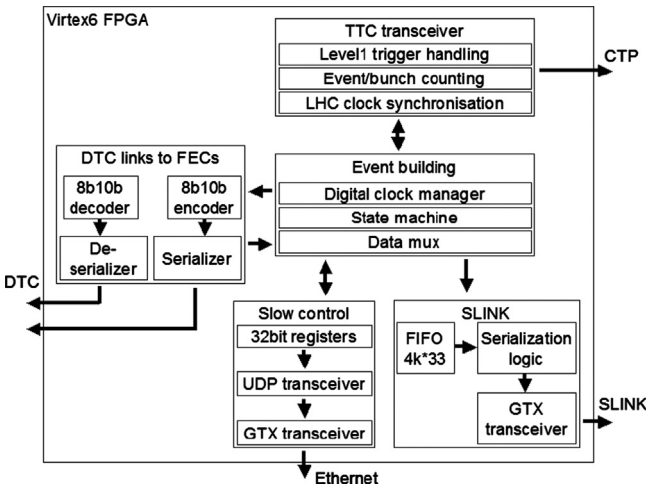

Fig. 2. Simplified block diagram of the SRU ROD firmware.

has recently been tested, showing no transmission errors during several days of running. The bit error rate is smaller than 10^{-12}.

3.3. Event building

Each event data must be formatted in a fixed way, to be compatible with the ATLAS data acquisition chain. The data format includes trigger-specific data like bunch-crossing ID and event-ID as well as run-specific parameters and of course the digitized charge values from the anode strips of the detectors. The event building algorithms work properly, all necessary information for a valid ATLAS event are included in the output frames.

3.4. Error correction

In its final design, the ROD firmware will check for possible errors in event data and error conditions, and mark the ATLAS frame accordingly.

3.5. SLINK transmission

Data are transmitted to the ROS PC using the standard ATLAS read-out link SLINK, sending 32 bit words with 40 MHz frequency over optical fiber with 2 GBit/s bandwidth. The RODs used in ATLAS require therefore a HOLA [4] daughter card, which accommodates a separate FPGA for protocol handling and a Texas

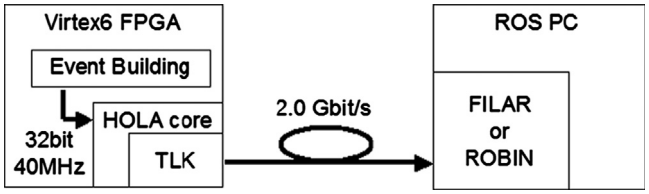

Fig. 3. Block diagram of the SLINK implementation.

Instruments TLK2501 IC [5] for data serialization/deserialization and encoding. The increased logic density of today FPGAs allowed to include the complete HOLA functionality in the SRUs Virtex6 FPGA, using one of its high-speed GTX transceivers and the onboard SFP+ slots with an optical plug (see Fig. 3). SLINK transmission using internal FPGA resources was tested successfully. The SRU has been connected to a ROS PC and valid event data were received with both FILAR and ROBIN pci cards, the latter used in the ATLAS ROS PCs.

3.6. Slow control

Run control, debugging and fine-tuning of different parameters are realized via optical Ethernet connection to the SRU. This also allows online firmware upgrades to the SRU's onboard BPI-Flash chip, where the SRU by default boots from. Online preview of the gathered raw data is especially important and useful during the commissioning of the ROD and all detector parameters, including the TTCrx and APV25 settings. The SRU firmware therefore has to forward all slow control frames for the FEC cards and APV25 chips via the DTC links.

4. Conclusion

The firmware development of an ATLAS ReadOutDriver for Micromegas detectors using the SRS system is in an advanced state. As soon as the TTC connectivity is realized, the ROD is able to be part of the ATLAS data acquisition chain. First tests within this framework are foreseen within the coming weeks.

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